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EXAMINER	
NGUYEN, HIEP	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,944	DRAPKIN ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8,9,11-19,21,23 and 25-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5, 6, 8, 9, 12, 13, 18, 19, 23, and 25-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 2, 12, 12, 13, 18, 19, 23, 26, 27, 30 and 31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 1, the recitation "introducing a current to said parasitic capacitance to compensate for current of said input signal charging said parasitic capacitance responsive to detection of a positive edge of said input signal" is indefinite because it is not clear how the current of the input signal is compensated.

Claims 12 and 13 are indefinite because they are confusing. In claim 12, when the edge of the input is positive, a current is introduced to the parasitic capacitance an in claim 13 when the edge of the input is positive, a current is prevented from introducing a current from the parasitic capacitance to the input signal. In conclusion, it is not clear how when the input signal has a positive edge, the circuit can perform two different functions.

Regarding claims 19 and 23, the recitation "the step of preventing discharge includes introducing the current to said input" is indefinite because it is misdescriptive. For preventing discharging into the input of the circuit, the current cannot be introducing into the input as recited.

Regarding claims 26, 27, the recitation " thereby eliminating a need for an additional parasitic capacitance to reduce distortion" is indefinite because a parasitic capacitance is not a discrete capacitance thus it cannot be added to the circuit.

Regarding claims 30 and 31, the recitation "wherein said detection circuit is independent of said mentioned circuit" is indefinite because it is not clear what "said mentioned circuit" is meant by. Assumed the "said mentioned circuit" is the circuit of claim 5 that comprises a "detection circuit" then the said detection circuit is not independent of said "mentioned circuit".

The Applicant is requested to point out what are the "said mentioned circuit" and the "detection circuit" in the drawing. Claims 2 and 18 are indefinite because of the technical deficiencies of claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5, 6, 8, 9, 12, 13, 23, 25, 26 and 28-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Bruccoleri et al. (US Pat. 5,808,488).

Regarding claims 1, 2, 18 and, figure 3 of Bruccoleri shows a method for reducing distortion of a signal to and input of an input/output device having parasitic capacitance (Cin) between said input and ground, comprising the step of:

detecting at said input a direction of change in voltage of the input signal applied to the input of inverter (INV1);

introducing a current to the parasitic capacitance to compensate for current of said input signal charging said parasitic capacitance responsive to detection of a positive edge of said input signal. Note that when the input signal voltage rises the parasitic capacitor (Cin) forming by the gate-source/drain of the transistor(s) of inverter (INV1) starts to be charged. When a rising edge of the input signal is detected to be higher than the input threshold, the output voltage of inverter (INV1) becomes low and the output of inverter (INV2) becomes high thus a current is introduced by the output of inverter (INV2) to the parasitic capacitor (Cin) to "compensate" for current of the input signal that charges the parasitic capacitor (Cin). The parasitic capacitance (Cin) exists across the input and the ground. The detection circuit comprises inverter (INV1) and the correction circuit is inverter (INV2). The levels of the input signal are detected at the input of inverter (INV1).

Regarding claims 3, 19 and 27, figure 3 of Bruccoleri shows a method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance between said input and ground, comprising the steps of:

detecting at the input (Z+) of said circuit a direction of change in voltage of said input signal; and

preventing discharge of said parasitic capacitance into the input of said circuit responsive to detection of a negative edge of said input signal. Note that when the input (Z+) is low (negative edge), the output of the correction circuit (INV2) is low thus, the parasitic capacitance is discharge via inverter (INV2) and the discharge of said parasitic capacitance into the input of said circuit is prevented.

Regarding claims 5, 6, 25 and 30, figure 3 Bruccoleri shows an apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance (Cin) between said input and ground, comprising:

a detection circuit (INV1) coupled to said input for detecting a change in voltage of said input signal (Vin+) coupled to said input; and

a correction circuit (INV2) coupled between said detection circuit and said input for compensating for current from said input signal diverted to said parasitic capacitance due to a positive edge of said input signal. It is inherent that the detection circuit (INV1) includes a capacitance directly connecting to one terminal of the parasitic capacitance.

Regarding claims 8, 9 and 31, figure 3 Bruccoleri shows an apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance (Cin) between said input and ground, comprising:

a detection circuit (INV1) coupled to said input for detecting a change in voltage of said input signal coupled to said input; and

a correction circuit (INV2) coupled between said detection circuit and said input for compensating for current from input signal due to a negative edge of said input signal. It is inherent that the detection circuit (INV1) includes a capacitance directly connecting to one terminal of the parasitic capacitance.

Regarding claims 12, 13 and 23, figure 3 Bruccoleri shows a method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance between said input and ground, comprising the steps of:

detecting at said input a direction in change (high or low) in voltage of said input signal;

and introducing a current from the output of the detection circuit (INV2) to said parasitic capacitance to compensate for distortion of said input signal due to said parasitic capacitance responsive to detection of a positive edge of said input signal. When the edge of the input signal is negative, the circuit prevents introduction of a current from the parasitic capacitance into the input signal.

Regarding claims 28 and 29, the detection (tracking) circuit (INV1) is isolated from the output (Vout+) by element (BF1).

Claims 1, 2, 5, 6, 12, 18, 25 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Diniz et al. (US Pat. 6,107,868).

Regarding claims 1, 2, 18, 12, 22 and 26, figure 3 of Diniz shows a method for reducing distortion of a signal to and input of an input/output device having parasitic capacitance, comprising the step of:

detecting at the input (the gate of transistor 48) a direction of change of the input voltage at the input;

introducing a current (64) when a positive edge of the input signal is applied to the gate of transistor (48) to charge the parasitic capacitance, not shown and inherently exists between the gate of and the source of transistor (48), to compensate the current of the input signal charging said parasitic capacitance.

Note that when the input signal voltage rises the parasitic capacitance forming between the gate-source/drain of the transistor (48) is charged. When a rising edge of the input signal is detected to be higher than the input threshold, transistor (48) is turned on and a current (64) is introduced to the parasitic capacitor to compensate for current of the input signal that charges the input parasitic capacitance. The input parasitic capacitance is considered to exist across the input terminal (the gate terminal of transistor 48) and the ground.

Regarding claims 5, 6 and 25, it is inherent that figure 3 of Diniz shows an apparatus for reducing distortion of a signal applied to an input of a circuit at high frequency a having parasitic capacitance, comprising: a detection circuit (48) for detecting changes of the input voltage; a correction circuit (44, 46, 49) coupled to the detection circuit for compensating the current from the input signal diverted to the parasitic capacitance, not shown, between the gate and the source of transistor (48), due to the positive edge of the input signal. Note that when the input signal voltage rises, the parasitic capacitance formed between the gate-source/drain of the transistor (48) is charged. When a rising edge of the input signal is detected to be higher than the input threshold, transistor (48) is turned on to activated transistor (46) and current (64) is generated to be introduced to the parasitic capacitance to compensate for current of the input signal that charges it. The parasitic capacitance is considered to exist across the input terminal (the gate of transistor 48) and the ground.

Response to Arguments

In page 12, 13, 14, 15, the Applicant argues that Bruccoleri fails to teach or even suggest an arrangement wherein the change in current is detected directly at the input of the circuit. In fact, Bruccoleri fully suggests an arrangement wherein the change in current is detected directly at the input of the circuit. Figure 3 of Bruccoleri clearly shows that the **detection circuit** (INV1) detects the change of current that is directly inputted to the input node (Z+) and generates a detection signal at its output. The correction circuit (INV2) receives this detection signal and generates a correction signal for introducing a current to compensate for current of the input signal charging the parasitic capacitance. Note that the in page 13 of the Remarks the Applicant argues that "In spite of this, it should be noted that the circuitry of Figure 3 directed to claims 3, 19, 13, 23 and 27 requires that the detection of a change of signal is obtained at the **output** of INV1, which is applied to the input of INV2 whose output is then coupled to the input of INVI". Figure 3 shows that the change of signal is directly obtained at the **input** of the detection circuit INV1 and the **result** of the detection is the output signal of (INV1). When a negative edge of the input signal is directly inputted to the input terminal (Z+), the output of the correction circuit (INV2) becomes LOW. As a result, the parasitic capacitance at the detection

circuit (INV1) is discharged via the output of the correction circuit (INV2) thus, the parasitic capacitance to be added to the input signal is compensated.

In page 16, last paragraph, the Applicant argues that "... This is a clearly **different arrangement** from that taught in the invention and it is submitted that claims 1, 2, 5, 6, 12 18, 25 and 26, all of which have been discussed above as containing limitations, or which depend from claims which contain limitations, of the detection taking place directly at the input of the circuit, patentably distinguish over both Diniz and Bruccoleri which detect changes in the input signal at the output (and not the input) of the "circuit."". It is true that the circuit of Diniz has an arrangement different than circuits of figure 2C of the present application but the circuit of Diniz is identical to the claimed circuit. The circuit of Diniz, figure 2 or figure 3 detects a signal directly applied to the input (the gate of transistor 48, having input parasitic capacitance). Depending in the positive or negative edge of the input signal, the parasitic capacitance is charged or discharged. When the input has a positive edge, transistor (48) is turned on and current (64) which is equal to current (66) is generated to compensate for the current of the input signal charging the parasitic capacitance. When the input has a negative edge (low level), transistor (48) is turned off. The parasitic capacitance is discharged via the circuit (72) thus, preventing discharge of said parasitic capacitance into the input of the circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
09-03-04

TUAN T. LAM
PRIMARY EXAMINER